a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap with a portion of said second conductive layer which is in contact with said gate insulating film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap with another portion of said second conductive layer which is in contact with said gate insulating film.

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6. (Amended) A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and a top surface and side surfaces of said first conductive layer;

Fig. 1

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap with a portion of said second conductive layer which is in contact with said gate insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to overlap with said second conductive layer;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap with another portion of said second conductive layer which is in contact with said gate insulating film.

11. (Amended) A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlap with said first gate electrode, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said third impurity region is disposed so as to partially overlap with said second gate electrode, and

wherein a wiring is electrically connected to said third impurity region.

14. (Amended) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap with a portion of said second conductive layer which is in contact with said gate insulating film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap with another portion of said second conductive layer which is in contact with said gate insulating film.

19. (Amended) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity

region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap with a portion of said second conductive layer which is in contact with said gate insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to overlap with said second conductive layer;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap with another portion of said second conductive layer which is in contact with said gate insulating film.

24. (Amended) A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlap with said first gate electrode, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a